Design and Analysis of a Class-D Stage with Harmonic Suppression

Jonas Fritzin, Student Member, IEEE, Christer Svensson, Fellow, IEEE,
Atila Alvandpour, Senior Member, IEEE

Abstract—This paper presents the design and analysis of a low-power Class-D stage in 90nm CMOS featuring a harmonic suppression technique, which cancels the 3rd harmonic by shaping the output voltage waveform. Only digital circuits are used and the short-circuit current present in Class-D inverter-based output stages is eliminated, relaxing the buffer requirements. Using buffers with reduced drive strength for the output stage reduces the 5th harmonic at the output, as the rise and fall time of the output voltage increase. Operating at 900MHz, the measured output power was +5.1dBm with Drain Efficiency (DE) and Power-Added Efficiency (PAE) of 73% and 59% at 1.2V. The 3rd and 5th harmonics were suppressed by 34dB and 4dB, respectively, compared to an inverter-based Class-D stage.

Index Terms—radio transmitter, CMOS, harmonic rejection

I. INTRODUCTION

WITH the improved speed of the CMOS transistors, highly efficient switched amplifiers, like Class-D and Class-E, have gained increased interest not only for constant envelope amplification, but also in linearization schemes like polar modulation and outphasing at radio frequencies [1]-[12]. While switched amplifiers may provide higher power efficiency compared to traditional linear amplifiers, they also generate strong harmonics in the output spectrum unless filtered out. In order not to contaminate the frequency spectrum, filters are used to suppress the harmonics in the output spectrum, and as the number of wireless standards grows, so does the number of filters. Therefore, suppression of the harmonics in the output spectrum, by not generating them in the RF amplifiers, could be an important step towards a more flexible transmitter structure covering multiple frequency bands. Harmonic rejection solutions for receivers have been proposed in [13]-[15]. Previous approaches on harmonic suppression in transmitter circuits include harmonic rejection mixers canceling 3rd and 5th harmonics [16], as well as multiphase [17] and polyphase multipath [18], [19] techniques. The polyphase multipath technique presented in [18], [19], used digital circuits and switched transconductor mixers in the output stage and utilized the circuit theory in [20]. The technique suppressed harmonics and sidebands to levels smaller than -40dBc up to the 17th order but with a low efficiency.

In this paper, we present the design and analysis of a low-power Class-D stage featuring a harmonic suppression technique [1]. The Class-D stage suppresses the 3rd harmonic in the output spectrum by shaping the drain voltage. Due to the switching scheme of the proposed Class-D stage, the short-circuit current is eliminated, relaxing the buffer requirements of the output stage. Using buffers with reduced drive strength for the output stage reduces the 5th harmonic at the output, as the rise and fall time of the output voltage increase. The proposed Class-D stage is suitable for constant envelope modulation, but can also be used in outphasing applications [1]. The design of outphasing amplifiers is further discussed in [21].

The paper is organized as follows. In section II, the operation of the proposed Class-D stage with harmonic suppression is explained. This section also covers the implementation and presents an analysis of the harmonic

Figure 1. a) Class-D inverter-based stage
b) Drain voltage waveform of the Class-D inverter-based stage

Figure 2. a) Proposed Class-D stage with harmonic suppression
b) Drain voltage waveform of the Class-D stage with harmonic suppression
contents of the output voltage. In section III, a performance comparison, based on simulations, of the proposed Class-D stage and an inverter-based Class-D stage is presented. In section IV, the measurements of the Class-D stage with harmonic suppression are presented, followed by conclusions in section V.

II. DESCRIPTION OF THE CLASS-D STAGE WITH HARMONIC SUPPRESSION

A. Operation of the Proposed Class-D Stage with Harmonic Suppression

Figure 1a shows an inverter-based Class-D stage, using a PMOS and an NMOS transistor, \( T_A \) and \( T_B \). Considering the square-wave drain voltage in Figure 1b, the closest and strongest harmonic compared to the fundamental tone is the 3rd harmonic, which is \(-9.5\text{dB} \) relative the fundamental tone. If the 3rd harmonic could be eliminated from the square-wave, the resulting waveform would look like the one in Figure 2b. This does not generate 2nd and 4th harmonics as long as the \( V_{DD} \) and ground portions of the drain voltage are symmetrical and positioned correctly in time. This means that the output spectrum of the output voltage in Figure 3 would be clean up to the 5th harmonic (-14dBc), which is also indicated by the Fourier coefficients in (1).

\[
b_n = \frac{V_{DD}}{n \pi} \left[ \cos \left( \frac{n \pi}{6} \right) - \cos \left( \frac{5n \pi}{6} \right) \right]
\]

To create the desired drain voltage (Figure 2b), two voltage sources and ground would be needed. Figure 2a shows the proposed Class-D stage with harmonic suppression, including one additional transistor (\( T_C \)) and a capacitor (\( C_C \)), which also eliminates the need for a second voltage source (\( V_{DD}/2 \)).

The operation of the Class-D stage is as follows. The three transistors in the output stage have separate drive signals (\( V_{drv} \)). The drain of the output stage can be pulled to \( V_{DD} \) through the PMOS transistor (\( T_A \)) or pulled down to ground via the NMOS transistor (\( T_B \)). When neither the transistor \( T_A \) nor the transistor \( T_B \) drives the drain node, the center transistor (\( T_C \)) connects the capacitor \( C_C \) to the drain node. Figure 4 shows the drive signals of the output stage. Transistor \( T_C \) is turned on twice per cycle.

Consider the case when transistor \( T_A \) has pulled the drain node to \( V_{DD} \) and charged the drain capacitance (\( C_d \)) to \( V_{DD} \). When \( T_A \) turns off, and \( T_C \) still is turned off, the drain capacitance starts to discharge via the load resistance \( R_L \). Once \( T_C \) is turned on, there is a charge redistribution between \( C_C \) and \( C_d \) such that the voltage across them becomes the same. Consequently, since the voltage \( V_C \) across \( C_C \) is lower than \( V_{DD} \), there will be a current going into the drain of \( T_C \) to charge \( C_C \) as illustrated in Figure 5a.

Similarly, we can consider the case when transistor \( T_B \) has pulled down the drain node to ground and discharged the drain capacitance. When \( T_B \) turns off, and \( T_C \) still is turned off, the drain capacitance starts to charge via the load resistance. Once \( T_C \) is turned on, the charge redistribution occurs again. However, this time there will be a current going out of the drain of \( T_C \) to discharge \( C_C \) as shown in Figure 5b. The \( C_C \) capacitor is alternately being charged and discharged. Due to the symmetry, the average current through \( T_C \) becomes zero when \( V_C \) has settled at \( V_{DD}/2 \). Therefore, the need for a
second voltage source of $V_{DD}/2$ is eliminated and can be replaced by a large capacitor $C_C$ as in the proposed Class-D stage.

The time needed for the charge redistribution to occur depends on the on-resistance of $T_C$. Too high on-resistance makes the transitions slower and affects the shape of the drain voltage. A sufficiently large capacitor $C_C (C_C \gg C_d)$ must be chosen to ensure a stable $V_C$ voltage during the charge and discharge periods of the drain capacitance. To further demonstrate the operation of the Class-D stage, ideal simulation results are shown in Figure 6. In the figure, the charge and discharge currents are clearly visible as well as the small changes in $V_C$ during charging and discharging of $C_C$.

B. Implementation of the Class-D Stage with Harmonic Suppression

Figure 7 shows the proposed Class-D stage with harmonic suppression including all buffers, designed and manufactured in a 90nm CMOS technology. The chip photo is shown in Figure 8 and includes the output stage, input buffers and the buffers for the output stage. The tapering factor $\lambda_0 = \lambda_n = \lambda_{nc}$ of the buffers was $\lambda = 3$. To be able to directly connect the Class-D stage to a spectrum analyzer and demonstrate the harmonic suppression technique, the amplifier was designed for a 50Ω load and optimized for power-added efficiency at 900MHz for a 1.2V supply. The drain efficiency (DE) includes the output stage, while the power-added efficiency (PAE) includes the output stage and the buffers of the output stage. The DC power to drive the buffers was considered as input power.

The target operation frequency 900MHz was chosen because of the low output power of the Class-D stage, and its suitability for the closely located European Short-Range Devices (SRD) 862-870MHz and the North American 902-928MHz Industrial Scientific & Medical (ISM) frequency bands.

The required drive signals of the output stage were shown in Figure 4, where the pulse widths for the transistors $T_A$ and $T_B$ were $4\pi/3$ and $2\pi/3$, respectively. The corresponding pulse width of the drive signal of transistor $T_C$ was $\pi/3$. The drive signal for transistor $T_C$ was generated using an XOR of the drive signals for $T_A$ and $T_B$. Two DC bias levels were applied together with the RF signal at the input of the input buffers to set the pulse widths of the input signals $V_{in1,XOR}$ and $V_{in2,XOR}$ of the XOR gate in Figure 7.

In the output stage, the transistor widths were 50μm ($W_{n0} = W_{n0}$) and 160μm ($W_{p0}$) with a nominal channel length of 0.1μm. The W/L (μm) ratio of the NMOS and PMOS transistors in the last buffer stage of $T_B$ was 2.92/0.1 and 8.76/0.1. The corresponding numbers for the $T_A$ and $T_C$ transistors were 8.76/0.1 and 26.3/0.1, and 4.2/0.1 and 12.5/0.1, respectively. The ratio of the transistor width in the output stage (e.g. $W_{n0}, W_{n0}$ and $W_{p0}$) divided by the sum of the transistor widths in the last buffer stage are for the $T_A, T_B$, and $T_C$ transistors approximately equal to 4.6 (160/(8.76+26.3)), 4.3 (50/(2.92+8.76)), and 3 (50/(4.2+12.5)). The $C_C$ capacitor was implemented as a 30pF MOS capacitor.

By adding a simple off-chip LC filter (L_filter, C_filter in Figure 7) with characteristic impedance of 50Ω a wideband matching is attained from DC up to the cut-off frequency of the filter. The filter provides filtering of higher order harmonics, and as shown in the measurement section, the harmonics are suppressed enough to meet the -30dBm requirement when operating at 900MHz [22]. The filter is specified in the measurement section.
C. Short-Circuit Current Elimination and Output Voltage Analysis

In inverters, the short-circuit power dissipation depends on the rise and fall times of the input signal [23]. In Class-D inverter-based amplifiers, this power dissipation may become important since the driver of an output stage typically is designed as an inverter chain with a tapering factor [2]. This results in finite rise and fall times on the output stage and will have a negative impact on the drain efficiency [2], [3], which is also shown in section III. Since transistors TA and TB in the proposed stage are never on simultaneously, there is no direct path between VDD and ground, and the short-circuit current in the output stage is eliminated. This property lowers the buffer requirement and makes it possible to use buffer stages with reduced drive strength for the output stage. Thus, the ratio of the transistor width in the output stage (e.g. W0, Wnc0, and Wp0) divided by the sum of the transistor widths in the last buffer stage can be larger than the tapering factor of the buffers (λ = 3), except for the buffer of TC due to the narrow pulses being processed. The transistor width ratios for the TA, TB, and TC transistors are approximately equal to 4.6, 4.3, and 3 (see also section II.B). However, the rise and fall time on the output voltage will increase, but with only a low impact on the fundamental tone while the 5th harmonic is reduced, as described below.

Figure 9a shows the desired output voltage together with different assumptions on the rise and fall times, tr,f. The rise and fall time are in this case measured between ±VDD/2 and 0 with a linear slope and the corresponding Fourier coefficients are found in (2).

\[
b_h = \frac{V_{DD}}{n \pi^2 t_{r,f}} \left[2 \cos \left(\frac{n \pi}{6} \sin \left(\frac{nt_{r,f}}{2}\right) \right) + \sin \left(\frac{n}{6} (5 \pi - 3t_{r,f})\right)\right] + \sin \left(\frac{n}{6} (5 \pi + 3t_{r,f})\right)
\]

The power of the harmonics is plotted in Figure 9b, for a 1.2V supply and a load resistance of 50Ω. The figure shows the 5th harmonic dropping about 3dB when the rise and fall times are increased to π/6 (8% of the period time). At the same time the fundamental tone is hardly affected, it drops only 0.1dB. If the rise and fall times are further increased to a theoretical maximum, i.e. tr,f is π/3, the drop of the 5th harmonic is even larger, while the fundamental drops in total about 0.4dB. Consequently, the output power is relatively insensitive to the rise and fall time on the output voltage. While the 5th harmonic is reduced, the 2nd, the 3rd, and the 4th harmonics are still absent in the output spectrum. Hence buffer stages with reduced drive strength can be used for the output stage since the short-circuit current is eliminated, with small impact on the output power. However, the tapering factor of the TC buffer is limited due to the narrow pulses being processed. This combined with the need to match the delays of the TA, TB, and TC drivers, may force all drivers to use smaller tapering factors. This would reduce power-added efficiency, especially at higher frequencies.

In Figure 9 it was assumed that the rise and fall times were the same. Figure 10a shows an example, where the fall time is ideal and the rise time is varied. The power of the harmonics in (3), plotted in Figure 10b, show that even for an ideal fall time and long rise time (tr = π/3), the 2nd and 4th harmonics are smaller than -27dBc. Similar results are achieved if only the rise and fall time of the output voltage for t > 0 are varied between π/3 and π/6. The resulting 2nd and 4th harmonics (h4 coefficients) are < -20dBc and the 5th harmonic is between -15dBc and -18dBc. The 3rd harmonic is not generated in any of the two examples.

\[
b_h = \frac{V_{DD}}{n \pi^2 t_{r,f}} \left[nt_{r,f} \cos \left(\frac{5n \pi}{6}\right) - 2 \cos \left(\frac{n \pi}{6}\right) \sin \left(\frac{nt_{r,f}}{2}\right)\right]
\]
Another situation is illustrated in Figure 11a, where the pulses are assumed to be misaligned from their ideal location with a deviation of $\Delta \alpha$ radians. The corresponding Fourier coefficients are found in (4) and the strength of the harmonics is plotted in Figure 11b. The figure shows that deviations from the ideal pulse location will increase the 2nd and 4th harmonics in the output spectrum. To maintain a harmonic level of -30dBc, a fraction of a radian (a few degrees) of misalignment is acceptable.

$$b_n = \frac{V_{DD}}{\pi n} \left[ \cos \left( n \left( \Delta \alpha + \frac{\pi}{6} \right) \right) - \cos \left( n \left( \Delta \alpha + \frac{5\pi}{6} \right) \right) \right]$$  \hspace{1cm} (4)

The amplifier in Figure 7 requires a sinusoidal input signal. By adjusting the DC bias levels, $V_{bias1}$ and $V_{bias2}$, of the input buffers, the pulse width of the input signals to the XOR gate is controlled. If the RF signal, $V_{RF}$, is a square-wave, $V_{in1,XOR}$ and $V_{in2,XOR}$ will be identical and $T_C$ will not be turned on and the Class-D stage will operate as a conventional inverter, increasing the 3rd harmonic in the output spectrum. Assuming the driver signals of $T_A$ and $T_B$ are not appropriately generated (e.g. by erroneous biasing levels of the RF inputs) when applying a sinusoidal signal, the pulse widths of the $+/V_{DD}/2$ portions may differ from $2\pi/3$ and results in degraded 3rd harmonic suppression. The pulse width of the $+/V_{DD}/2$ portions is denoted $\psi$ as shown in Figure 12a and has the corresponding Fourier coefficients as in (5). Figure 12b shows the harmonic strength as a function of pulse width. Thus, with an inadequate quality of the input signal (deviations from a sinusoidal signal) or erroneous biasing of the input buffers, the generation of the driver signals for the output stage is affected, having an impact on the harmonic suppression at the output.

$$b_n = \frac{2V_{DD}}{\pi n} \sin \left( \frac{n\pi}{2} \right) \sin \left( \frac{n\psi}{2} \right)$$  \hspace{1cm} (5)

As $\psi$ is $2\pi/3$, the 3rd harmonic is eliminated and the first harmonic visible in the output spectrum is the 5th. Increasing the pulse width to $\pi$ (square-wave Class-D), the fundamental tone increases about 1.2dB while the 3rd harmonic becomes -9.5dBc.

Consequently, while finite rise and fall times as well as the pulse width time alignment do not degrade the suppression of the 3rd harmonic, it is important to ensure that the $+/V_{DD}/2$ portions of the output voltage have the desired pulse widths. Also, if the pulses are not correctly positioned in time, the 2nd and 4th harmonics will distort the spectrum as shown in Figure 11b.

If the delays in the driver stages are not matched, it may happen that both $T_A$ and $T_C$, or $T_B$ and $T_C$, are on at the same time. With non-ideal driver signal alignment, the symmetrical operation of the Class-D stage is disturbed and the voltage across $C_C$ will not be $V_{DD}/2$. If $T_A$ and $T_C$ are on at the same time as in Figure 13, both $C_C$ and $V_{DD}$ will be connected to the drain. $V_{DD}$ will then charge both $C_C$ and $C_C$, and increase the voltage across $C_C$ to a value around 650mV. Similarly, if $T_B$ and $T_C$ are on at the same time as in Figure 14, both $C_C$ and $GND$ will be connected to the drain. Then $C_C$ will start to discharge to $GND$ and the voltage across $C_C$ decreases to a value around 275mV. In simulations, this effect introduced asymmetries in the ideal drain voltage waveform, increasing the harmonic contents. Moreover, the output power and the DE were reduced by approximately 10%.

### III. SIMULATION COMPARISON BETWEEN THE PROPOSED CLASS-D STAGE AND AN INVERTER-BASED CLASS-D STAGE

#### A. Comparison between the proposed Class-D stage and the inverter-based Class-D stage

To compare the performance of the proposed Class-D stage with harmonic suppression to an inverter-based Class-D stage, two simulation models were evaluated at 900MHz. In the simulation model of the inverter-based amplifier a single buffer with four stages was used for the output stage. The tapering factor was set to 3 (as in the proposed Class-D stage), and the output stage had the same transistor sizes as $T_B$ and $T_A$. The simulated performance of both amplifiers is summarized in Table I. In the measurement section it is

---

**Figure 13.** The simulation results due to on-time overlap of $T_A$ and $T_C$.

**Figure 14.** The simulation results due to on-time overlap of $T_A$ and $T_C$. 
shown that the simulated performance of the proposed Class-D stage corresponds very well to the measured performance.

The output power of the proposed Class-D stage was 0.9dB lower than the output power of the inverter-based stage. This could be expected by considering the fundamental tone (n = 1) of the Fourier coefficients of a square-wave in (6), and the Fourier coefficients of the proposed Class-D stage in (1). Theoretically, the output power of the proposed Class-D stage, compared to the inverter-based Class-D stage, is approximately 1.2dB lower. Thus, there is a trade-off between peak output power and suppression of the 3rd harmonic.

\[ b_{n,\text{square}} = \frac{V_{DD}}{n \pi} \left( 1 - (-1)^n \right) \]  

(6)

The 3rd harmonic was approximately -10dBc in the simulated output spectrum of the inverter-based stage, as expected according to (6). In the output spectrum of the proposed Class-D stage the 3rd harmonic was suppressed about 30dB compared to an inverter-based Class-D stage. The simulated power gain, from the input of the buffers to the output, was 25dB for both cases. The DC power to drive the buffers was considered as input power.

The simulations show that the proposed Class-D stage had a higher DE and PAE despite lower output power, larger number of buffer stages, and larger gate and drain capacitances in the output stage due to \( T_C \). The simulation results can be explained by a number of factors described below.

As already discussed, the short-circuit power dissipation is eliminated in the proposed Class-D stage. In the simulations of the inverter-based Class-D stage, two simulations were performed to extract the short-circuit power dissipation. In the first simulation, non-overlapping driver signals were used for the output stage and from the total power dissipation it was possible to compute how much power was dissipated in the load (considering all harmonics) and the power consumption due to charging/discharging of \( C_d \). In the second simulation, the inverter-based Class-D was simulated with an overlapping driver signal, i.e. a single buffer was used. As the power consumption due to \( C_d \), known, the short-circuit power can be compared. In simulations, the short-circuit power dissipation of the inverter-based stage represented approximately 6% of the total power dissipation in the output stage, having a negative impact on the drain efficiency.

Furthermore, an inverter-based Class-D amplifier with a square-wave output voltage requires an optimal filter in terms of an ideal series resonator in series with the load to achieve 100% drain efficiency [24]. Considering the harmonic contents of an unfiltered inverter-based output stage, the drain efficiency drops to 81%, as in (7), as the harmonics will also be dissipated in the load.

\[ \left( \frac{b_{n,\text{square}}}{n} \right)^2 \sum_{n=1}^{\infty} \left( \frac{b_{n,\text{square}}}{n} \right)^2 \approx 0.81 \]  

(7)

Consequently, since the 3rd harmonic is not generated at the output of the proposed Class-D stage and do not consume any power, the maximum theoretical drain efficiency is increased to 91% (8) without any filtering requirement. In (8), \( b_n \) are the Fourier coefficients in (1) for the output voltage in Figure 3.

\[ \frac{k^2}{\sum n^2 k_n^2} = 0.91 \]  

(8)

When adding transistor \( T_C \) in the proposed output stage, the drain capacitance is increased by approximately 25% compared to the inverter-based stage (assuming \( W_{dc} = W_{nc0} \), \( W_{pi} = 3 \times W_{ao} \)). This has a negative impact on the drain efficiency, but this effect is mitigated by the stepwise charging in the proposed Class-D stage as discussed in section II.A. Assuming \( V_C \) is zero at startup, the supply voltage needs to charge the drain capacitance from 0 to \( V_{DD} \). Steady-state, i.e. when \( V_C = V_{DD}/2 \), is reached after 30 cycles. In steady-state, i.e. when \( V_C = V_{DD}/2 \), the supply voltage needs to charge the drain capacitance from \( V_{DD}/2 \) to \( V_{DD} \). Therefore, the theoretical dynamic power dissipation due to \( C_d \) can be reduced by 50% compared to an inverter-based stage [25]. In simulations of the proposed Class-D stage, the power dissipation was reduced by approximately 35%. Thus, while an increase of the drain capacitance increases the power consumption, the stepwise charging reduces the power consumption in the proposed Class-D stage. \( P_1 \) in (9) represents the power consumption due to switching of a drain capacitance, \( C_d \), between ground and \( V_{DD} \), at a frequency, \( f \), in the inverter-based Class-D stage. The corresponding power consumption in the proposed Class-D stage is represented by \( P_2 \) in (10).

\[ P_1 = C_d V_{DD}^2 f \]  

(9)

\[ P_2 = \frac{(1.25C_d)(1 - 0.35)W_{ao}^2 f}{f} = 0.81 C_d V_{DD}^2 f \]  

(10)
Thus, the power consumption in the proposed Class-D stage is 19% (1-0.81) lower compared to the power consumption in the inverter-based Class-D stage.

To achieve higher output power from the proposed Class-D stage, the transistors need to be larger to reduce their on-resistance and $R_L$ in Figure 7 must be made smaller. The impedance transformation of $R_L$ can also be achieved by using the LC filter as an L match. Here it is assumed that the impedance transformation is lossless.

Increasing the transistor sizes by a factor ‘k’, the on-resistance reduces and $C_d$ increases with the same factor. Simultaneously, if the load resistance $R_L$ is reduced by a factor ‘k’, the output power will be higher with a factor ‘k’. Thus, the output power increases as much as the power consumption due to charging/discharging of $C_d$ does increase, which means that the DE is maintained. This was verified in simulations and is summarized in Table II, demonstrating that the proposed Class-D stage can be used for higher output power without degrading efficiency. Similarly, PAE will be maintained as the transistors in the buffers are scaled with a factor of ‘k’ (assuming the transistor ratios are maintained).

B. The impact of LC filter

As the proposed circuit does not cancel the 5th and higher order harmonics, there is a need to filter out these harmonics in a real application with emission restrictions, here considering low-power transceivers operating in the 900MHz band [22]. Figure 15 shows the Class-D stage modeled as an ideal voltage source, $V_{source,n}$ together with an equivalent series on-resistance, $r_{on}$ and drain capacitance, $C_d$ [26], [27]. A transfer function from $V_{source,n}$ to the output voltage, $V_{out}$, can be found as in (11). $V_{source,n}$ is a voltage source with a fundamental tone (n = 1) and a large number of harmonics, whose amplitudes are determined by the Fourier coefficients in (1). Therefore, ideally, the proposed Class-D stage behaves as an inverter-based Class-D stage but with three discrete voltage levels; $V_{DD}$, $V_{DD}/2$ and $G_{ND}$, whose output spectrum lacks the 3rd harmonic.

$$H(j\omega) = \frac{V_{out}}{V_{source,n}} = \frac{R_L}{(r_{on} + R_L) - \omega^2 L_{filter} + j\omega L_{filter} + C_{filter} R_L + C_d r_{on} + jC_d R_L}$$

It should be noted that, using an inductive load and non-overlapping drive signals for the $T_{A}$-$T_{C}$ devices can cause the drain voltage to deviate from the ideal drain voltage waveform as the inductor acts as a short-term current source when none of these devices are turned on and will charge/dischARGE the parasitic at the drain. This can result in increased harmonic contents at the drain, but the harmonics can be suppressed by the frequency characteristics of the load (here the LC filter), which is also demonstrated in section IV and Figure 18.

$$Z_0 = \sqrt{\frac{L_{filter}}{C_{filter}}} \quad \omega_c = \frac{1}{\sqrt{L_{filter} C_{filter}}} \quad (12)$$

By choosing the characteristic impedance, $Z_0$, of the filter equal to the load resistance, $R_L$, as in (12), a wideband match is achieved from DC to the cut-off frequency, $\omega_c$, of the filter.

Since many low-power medical applications transmit in the 400 and 900MHz bands, two suitable filters are simulated with cut-off frequencies at 500 (dashed) and 1000 (solid) MHz with the characteristics as in Figure 16. The power of the fundamental tone in simulations without filter was 3.5mW (+5.5dBm), and since the 5th harmonic will be -14dBc, it is necessary to suppress the 5th harmonic by 22dB (6-14-22 = -30dBm) to comply with the emission requirements for low-power transceivers operating in the 900MHz band [22]. Considering the two filter characteristics of the two simple LC filter one can see that the suppression at 2GHz (5 x 0.4GHz) and 4.5GHz (5 x 0.9GHz) is about 24 and 26dB. Thus, when operating at 900MHz, the 5th harmonic will be suppressed to -34dBm (6-14-26 = -34dBm or -40dBc), which is acceptable according to the requirements in [22] and proves that simple LC filters can provide sufficient suppression in Class-D PAs as long as the 3rd harmonic is eliminated. This is also verified in the measurement section.

IV. MEASUREMENT RESULTS

A. Measurements of the Proposed Class-D Stage with Harmonic Suppression

Figure 8 showed the chip photo of the proposed Class-D stage manufactured in a 90nm CMOS technology. The area of
a single Class-D stage was 0.012 mm² and includes the area of the transistors and the Cₖ capacitor. The chip was directly bonded onto a FR4 PCB and connected with bond-wires. In the measurements including the LC filter in Figure 7, two lumped components were used (L₅ = 5.6 nH, C₅ = 2.7 pF). The filter had a cut-off frequency of ~1 GHz, when taking into account the impact of the PCB traces.

Figure 17a and Figure 17b show the transient voltage measurements without filter at 400 MHz and 900 MHz, respectively, demonstrating the operation of the Class-D stage. The DC level is 0 due to the DC blocking capacitor in series with the 50 Ω load. No adjustments of the DC bias levels, V₃ and V₄, were made at 400 MHz and 900 MHz. Operating at 900 MHz without filter, the output power was +5.1 dBm with a DE and PAE of 73% and 59%, respectively. The power gain was 24 dB from the buffers of the output stage to the output. The DC power to drive the buffers was considered as input power. The Class-D stage had a 3 dB bandwidth of 2.5 GHz (0-2.5 GHz).

The harmonic contents of the proposed Class-D stage was evaluated using an FSK modulated signal (f_deviation = 50 kHz, 50 kbit/s) at 900 MHz [28]. Figure 18 shows the peak-hold spectral measurement up to 5 GHz for a resolution bandwidth (RBW) of 1 MHz. Measurements with and without filter are plotted together, where the harmonics are marked with circles. Without filtering, the 2nd to 4th harmonics were measured to be smaller than -37 dBc and below -30 dBm [22]. The 3rd harmonic was -38 dBm (-43 dBc). The 5th harmonic was -13 dBm (-18 dBc), which corresponds well to the theoretical analysis with a suppression of a few dB of the 5th harmonic as the rise and fall times are increased as in Figure 17b. Thus, the 3rd and 5th harmonics were suppressed by 34 dB and 4 dB, respectively, compared to an inverter-based Class-D stage.

Operating at 900 MHz with filter, the output power was +5.3 dBm with a DE and PAE of 62% and 52%, respectively. The filter suppressed all harmonics to levels below -40 dBm except for the 5th harmonic, which had a strength of -36 dBm (-41 dBc) and corresponds well to the theoretical analysis in
Section III.B. In measurements with and without filter, the 3rd harmonic was suppressed more than 30dB compared to an inverter-based Class-D stage which means a power level below -34.4dBm (<-34.4dBm = +5.1dBm ~9.5dB ~30dB). The measured performance is summarized in Table III.

Operating at 400MHz without filter, the output power was +4.7dBm with a DE and PAE of 69% and 62%, respectively. The 2nd to 5th harmonics were measured to be -37dBc, -42dBc, -37dBc, and -14dBc, respectively.

B. Comparison with Other Work

In [18], [19], a polyphase multipath technique was presented, which provided harmonic rejection up to the 17th harmonic by using digital circuits and switched transconductor mixers in the output stage. Figure 19 shows the principle of the harmonic rejection technique presented in [18] and [19]. The input signal, x(t) operating at the frequency ω, is injected into N equal nonlinear circuits. Before and after each nonlinear circuit an equal but opposite phase is applied as in (13), and by connecting all circuit outputs the unwanted harmonics are cancelled at the output, y(t). The harmonics not cancelled are the ones in (14). With the large number of devices in the output stage, the DE is limited to 11%.

\[ \phi_j = 360(j-1)/N, j = 1, 2, 3,..., N \]  
\[ (PN + 1)\alpha, P = 0, 1, 2, 3... \]  
\[ (13) \]  
\[ (14) \]

In [18], [19], a 9x higher input carrier frequency, compared to the output carrier frequency, is needed. In the proposed Class-D stage, only the carrier frequency is required, which reduces the complexity and the power consumption. The harmonics suppression was better in [18], [19], but the DE becomes about seven times higher in the proposed Class-D stage. The comparison is summarized in Table IV.

V. CONCLUSIONS

This paper has presented the design and analysis of low-power Class-D stage featuring a harmonic suppression technique, which cancels the 3rd harmonic. The technique creates a voltage level of \( V_{in}/2 \) from a single supply voltage to shape the drain voltage. Only digital circuits are used and the short-circuit current present in Class-D inverter-based output stages is eliminated, relaxing the buffer requirements. Using buffers with reduced drive strength for the output stage reduces the 5th harmonic at the output, as the rise and fall time of the output voltage increase. Operating at 900MHz, the measured output power is +5.1dBm with a Drain Efficiency (DE) and Power-Added Efficiency (PAE) of 73% and 59% at 1.2V supply. The 3rd and 5th harmonics were suppressed by 34dB and 4dB, respectively, compared to an inverter-based Class-D stage.

REFERENCES


[22] ETSI EN 300 220-1, v2.2.1, (2008-04)


Jonas Fritzin received his M.S. degree in electrical engineering from Chalmers University of Technology, Göteborg, Sweden, in 2004. Since February 2007, he has been a Ph.D. student in the Electronic Devices research group of the Department of Electrical Engineering, Linköping University. His research interests include Multi-Standard, High Power-Efficiency RF Power Amplifiers and Transmitters.

Christer Svensson (M’97–F’03) was born in Boras, Sweden, in 1941. He received the M.S. and Ph.D. degrees from Chalmers University of Technology, Gothenburg, Sweden, in 1965 and 1970, respectively. From 1965 to 1978, he was with Chalmers University of Technology, where he researched on MOS transistors, nonvolatile memories, and gas sensors. Since 1978, he has been with the Department of Electrical Engineering, Linköping University, Linköping, Sweden, where since 1983, he has been a Professor of electronic devices. He initiated a new research group on integrated-circuit design. He pioneered the fields of high-speed CMOS design in 1987 and low-power CMOS in 1993. He founded several companies, for example, Switchcore (publ.) and Coresonic, where he also serves as the Director. He has published more than 180 papers in international journals and conferences. He is the holder of 15 patents. His present interests include high-performance and low-power analog and digital CMOS circuit techniques for computing, wireless systems, and sensors. Dr. Svensson is a member of the Royal Swedish Academy of Sciences and the Royal Swedish Academy of Engineering Sciences. He was the recipient of the Solid-State Circuits Council 1988–1989 Best Paper Award.

Atila Alvandpour (M’99–SM’04) received the M.S. and Ph.D. degrees from Linkoping University, Sweden, in 1995 and 1999, respectively. From 1999 to 2003, he was a senior research scientist with Circuit Research Lab, Intel Corporation. In 2003, he joined the department of Electrical Engineering, Linköping University, as a Professor of VLSI design. Since 2004, he is the head of Electronic Devices division. He is also the coordinator of Linköping Center for Electronics and Embedded Systems (LINCE). His research interests include various issues in design of integrated circuits and systems in advanced nanoscale technologies, with a special focus on efficient analog-to-digital data converters, wireless transceiver front-ends, sensor interface electronics, high-speed signaling, on-chip clock generators and synthesizers, low-power/high-performance digital circuits and memories, and chip design techniques. He has published about 100 papers in international journals and conferences, and holds 24 U.S. patents. Prof. Alvandpour is a senior member of IEEE, and has served on many technical program committees of IEEE and other international conferences, including the IEEE Solid-State Circuits Conference, ISSCC, and European Solid-State Circuits Conference, ESSCIRC. He has also served as guest editor for IEEE Journal of Solid-State Circuits.