A +32 dBm 1.85 GHz Class-D Outphasing RF PA in 130nm CMOS for WCDMA/LTE

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Abstract—This paper presents a Class-D outphasing RF Power Amplifier (PA) which can operate at a 5.5 V supply and deliver +32 dBm at 1.85 GHz in a standard 130nm CMOS technology. The PA utilizes four on-chip transformers to combine the outputs of eight Class-D stages. The Class-D stages utilize a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5 V supply in the 1.2/2.5 V 130nm process without excessive device voltage stress. Spectral and modulation requirements were met when a WCDMA and an LTE signal (20 MHz, 16-QAM) were applied to the outphasing PA. At +28.0 dBm channel power for the WCDMA signal, the measured ACLR at 5 MHz and 10 MHz offset were -38.7 dBc and -47.0 dBc, respectively. At +24.9 dBm channel power for the LTE signal, the measured ACLR at 20 MHz offset was -34.9 dBc. To the authors’ best knowledge, the PA presented in this work has a 3.9 dB higher output power compared to published CMOS Class-D RF PAs.

Index Terms—outphasing, CMOS, power amplifier.

I. INTRODUCTION

With the scaling of CMOS transistors, the speed of the transistors increases while they are also being operated at lower supply voltages. Due to the lower supply and breakdown voltages it becomes more challenging to meet the requirement on output power, linearity, and efficiency in Power Amplifiers (PA). With the improved speed of CMOS transistors, highly efficient switched PAs, like Class-D and Class-E, have gained increased interest in polar modulation and outphasing [1]–[4]. In the outphasing amplifier, an input signal containing both amplitude and phase modulation is divided into two constant-envelope phase-modulated signals. The two signals are separately amplified by efficient switched amplifiers and connected to a power combiner, whose output is an amplified replica of the input amplitude and phase modulated signal.

The output power of CMOS Class-D RF PAs has, so far, been lower than +30 dBm [1]–[3]. This can partly be explained by that, for a given supply voltage and load resistance, the output power from a Class-D PA is theoretically several dB lower compared to other classes of PAs, like linear Class-A/B PAs. To achieve higher output power, either a high supply voltage can be used to obtain high voltage swing or a low load impedance, i.e. a high impedance transformation ratio, is needed. Using a high impedance transformation ratio can result in low efficiency, especially when matching networks are integrated on-chip, and bandwidth reduction [5]. A higher voltage swing can be achieved in Class-D PAs by utilizing cascoding techniques to be able to operate at two or three times the transistors’ nominal supply voltage [1]–[3], [6]. In [1]–[3], the voltage stress on the devices is limited to the nominal supply voltage by using two supplies in the output stage and in the drivers, i.e. $2 \times V_{DD}$ and $V_{DD}$ as shown in Fig. 1(a).

This paper presents a +32 dBm outphasing PA based on a Class-D stage, that utilizes a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5 V, $V_{DD}$, supply in the 1.2/2.5 V 130nm process without excessive device voltage stress. Fig. 1(b) shows the proposed Class-D stage. The low-voltage driver operates at a 1.3 V, $V_{DD}$1, supply. Thus, two independent voltage supplies are used in this work, i.e. $V_{DD1}$ and $V_{DD2}$. By driving all transistors in the cascode configuration it is possible to achieve a low on-resistance in the on-state, and distribute the voltage stress on the devices in the output amplifiers.
off-state. Consequently, with the flexibility of two independent voltage supplies it is possible to use a high supply voltage in the output stage to achieve a high output power, while also controlling the voltage stress on the devices.

The outphasing PA utilizes four on-chip transformers to combine the outputs of eight Class-D stages as shown in Fig. 2.

The outline of the paper is as follows. In Section II, the design of the Class-D stage, the outphasing RF PA and the transformer are presented. Moreover, the reliability considerations and the stress on the devices are discussed. In Section III, the measured RF performance and the performance for modulated signals are presented and compared with other work. In Section IV, the conclusions are provided. 

II. DESIGN OF THE CLASS-D STAGE AND THE OUTPHASING RF POWER AMPLIFIER

A. Design and Operation of the Class-D Stage

The Class-D stages, denoted PA in Fig. 1(b) and Fig. 2, operate with a high supply voltage of 5.5 V, $V_{DD2}$, and utilize cascoded devices. The transistors used are 1.2 V thin-oxide devices, $T_1$ and $T_4$, and 2.5 V thick-oxide devices, $T_2$ and $T_3$, with oxide thickness of 2.0 nm and 5.0 nm, respectively. The gates of $T_1$ - $T_4$ are separated from the driver stage by AC coupling capacitors, $C_1$ - $C_4$, and individually biased via two off-chip resistors as in Fig. 3(a). All transistors are driven by an AC-coupled low-voltage driver operating at 1.3 V, $V_{DD1}$. Fig. 4(a) shows the principle of the operation, where the gate voltages, $V_{g,1}$ - $V_{g,4}$, of the four transistors and the output voltage, $V_{out}$, of the Class-D PA stage are plotted together. Fig. 4(b) shows the cascode of the NMOS transistors and associated voltages. The gate bias levels of $T_1$ - $T_4$ are assumed to be $V_{DD2} - V_{DD1}/2$, $V_{DD2}/2 + V_{DD1}/2$, $V_{DD2}/2 - V_{DD1}/2$, and $V_{DD1}/2$, respectively.

When the output signal from the driver, $V_x$, in Fig. 1(b), is high, the gate voltage of $T_3$ is raised above the bias level such that $V_{g,3}$ becomes $V_{DD2}/2$, which reduces the on-resistance of $T_3$. When the output signal from the driver, $V_x$, is low, the gate voltage of $T_3$ is lowered below the bias level such that $V_{g,3}$ becomes $V_{DD2}/2 - V_{DD1}$. This lowers $V_{ds,4}$ and $V_{ds,4}$ to approximately $V_{g,3} - V_{i,3}$ (the threshold voltage of $T_3$) if subthreshold conduction is neglected, but also increases $V_{gs,3}$ and $V_{ds,3}$. The operation of $T_1$ and $T_2$ is the same, but they are in their on-state (off-stage) when $T_3$ and $T_4$ are in their off-state (on-stage).

Consequently, by choosing suitable bias points and driving all transistors with a low-voltage driver, the voltage stress on the devices can be suitably distributed during the whole RF-cycle and a high supply voltage can be used. If only $T_1$ and $T_4$ are driven by the low-voltage driver, either a lower $V_{DD2}$ or fixed bias levels $> V_{DD2}/2 + V_{DD1}/2$ for $T_2$ (or $< V_{DD2}/2 - V_{DD1}/2$ for $T_1$) must be used, which would reduce the output power. The voltage stress is further discussed in Section II-B.

To decouple $V_{DD2}$, MIM capacitors with a breakdown voltage of 10 V were used. The low-voltage driver of the output stage is a tapered buffer with tapering factor $\lambda = 2.5$. The transistor widths of $T_1$ - $T_4$ in Fig. 1(b) were 5 mm, 5 mm, 2 mm, and 2 mm, respectively. The channel lengths of the thin-oxide, $T_1$ and $T_4$, and thick-oxide, $T_2$ and $T_3$, devices are 0.13 $\mu$m and 0.28 $\mu$m, respectively. The bulks and N-wells are connected to $G_{ND}$ and $V_{DD2}$, respectively.

B. Reliability Considerations

The reliability of CMOS transistors due to oxide degradation is especially important to consider in circuits with large voltage swings, like PAs. As discussed in [7], [8], the impact of RF stress is not as damaging as DC stress. Two major degradation mechanisms in CMOS devices are Fowler-Nordheim tunneling, due to high electric fields across the gate oxide, and Hot Carriers (HC), i.e. accelerated carriers in the channel [9].

During RF operation, the Time-Dependent Dielectric Breakdown (TDDB) is proportional to the root mean square (rms) value of the electric field applied to the gate oxide [10], [11]. In [10], the transistors had similar time to failure when rms RF and DC stress experiments were compared. In simulations of the proposed Class-D stage, the rms electric fields between gate-drain, gate-source, and gate-bulk are $< 0.7$ V/nm gate oxide, which is expected to result in a lifetime of more than 10 years [9].

HC stress typically occurs when the drain-source voltage is larger than maximum rated $V_{ds}$ while $V_{gs}$ is at least half the drain-source voltage [11]. Sign of HC stress is for example increased threshold voltage, degrading PA performance. In the PA, presented in this paper, $V_{ds}$ is high ($\leq 1.5 \times V_{DD,nominal}$)
when the transistors are in their off-state and $V_{gs}$ is close to 0 V, thus minimizing the HC stress [6], [11]. Also, the simulated $V_{ds}$ of the proposed Class-D stage is smaller compared to Class-AB PAs, where the cascode device is typically not driven by the driver and $V_{ds}$ approaches $2 \times V_{DD,nominal}$ [11].

The drain/well breakdown of the 130nm process is 10 V. As the drain voltage of the proposed Class-D stage never exceeds $V_{DD}$, this breakdown voltage is never exceeded.

### C. Design of the Outphasing RF PA

Fig. 2 showed the implemented outphasing PA. In order to achieve a high voltage swing and high output power, the outputs of eight amplifiers are combined by using four transformers, $TR_1$-$TR_4$, with a 1:1 turns ratio. The secondary windings are connected in series. Two primary windings connect outputs between $s_1^+$($t$) and $s_2^-(t)$, and the other two primary windings connect outputs between $s_1^-(t)$ and $s_2^+(t)$ [2]. With this connection, the load impedance seen at the primary side of each transformer becomes $R_L/4$ (at maximum output power) [12]. At power back-off, the load impedance increase and the matching network losses are reduced [2]. Tuning capacitors were placed at the primary winding of the transformers to reduce the losses between the primary and secondary windings [13].

### D. Transformer Design

The seven-metal stack of the 130nm process, does not contain thick metal layers (> 2.5 μm) and limits the quality factors, $Q$, of the transformer windings. To improve $Q$ and handle the large currents, the traces were made wide. To get a good coupling factor, an overlay structure (i.e. stacked conductors) was used [13]. However, wide traces increase the parasitic capacitances and limit the number of turns in the windings. Therefore only transformers with a 1:1 turns ratio were used as shown in Fig. 3(b). Under the four transformers, $TR_1$-$TR_4$, floating metal shields were placed in $M_1$ and $M_2$ to reduce the losses [14]. This layout, does not require an explicit on-chip ground connection, which is typically challenging to design when using a grounded shield [14].

The primary windings of $TR_1$-$TR_4$ were implemented in $M_5$ and $M_6$ with total thickness and width of 1.2 μm and 30.0 μm, respectively. The secondary winding was placed in the top metal ($M_7$) with thickness and width of 0.9 μm and 40.0 μm, respectively. The self-inductances of the galvanically isolated primary windings, $L_p$, and equivalent secondary winding, $L_s$, (four series-connected secondary windings) were 0.5 nH and 1.8 nH, respectively. At 1.9 GHz, the quality factors, $Q_p$ and $Q_s$, were approximately 8 and 5, respectively. In EM simulations, the loss of a single transformer was 1.6 dB.

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**TABLE I**

<table>
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<tr>
<th>Ref., Year</th>
<th>$P_{out}$ [dBm]</th>
<th>$V_{DD}$ [V]</th>
<th>DE [%]</th>
<th>PAE [%]</th>
<th>$f$ [GHz]</th>
<th>Tech. [nm]</th>
<th>BW [GHz]</th>
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<tr>
<td>[4] 2010</td>
<td>+21.6</td>
<td>1.9</td>
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<td>52.0</td>
<td>1.92</td>
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<td>+25.1</td>
<td>2.0</td>
<td>-</td>
<td>40.6</td>
<td>2.40</td>
<td>32</td>
<td>1.0</td>
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<tr>
<td>[3] 2011</td>
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<td>2.5</td>
<td>-</td>
<td>55.2</td>
<td>2.25</td>
<td>90</td>
<td>1.0</td>
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<td>2.4</td>
<td>-</td>
<td>19.7</td>
<td>2.28</td>
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This work +32.0 5.5 20.1 15.3 1.85 130 0.95

(a) 1 dB bandwidth (BW)
(b) 3 dB bandwidth (BW)

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**TABLE II**

<table>
<thead>
<tr>
<th>Standard</th>
<th>Parameter</th>
<th>Measured</th>
<th>Required</th>
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<td>WCDMA</td>
<td>ACLR @ 5 MHz [dBc]</td>
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<td>-33</td>
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<td></td>
<td>ACLR @ 10 MHz [dBc]</td>
<td>-47.0</td>
<td>-43</td>
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<td>LTE</td>
<td>ACLR @ 20 MHz [dBc]</td>
<td>-34.9</td>
<td>-30</td>
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<td></td>
<td>EVM [%]</td>
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<td></td>
<td>Channel power [dBm]</td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td>+24.9</td>
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</tbody>
</table>

(a) 16-QAM modulation
A measured RF performance

Fig. 7 shows the chip photo of the PA implemented in a 130nm CMOS process. The chip was attached to an FR4 PCB and connected with bond-wires. Two R&S SMBV100A signal generators with phase-coherent RF outputs and maximum IQ sample rate of 150 MHz were used in the measurements.

Fig. 5 and Fig. 6 show the measured output power \( P_{\text{out}} \), drain efficiency (DE), and power-added efficiency (PAE) over frequency and outphasing angle, \( \phi \), for \( V_{DD1} = 1.3 \) V and \( V_{DD2} = 5.5 \) V. At 1.85 GHz, the output power was +32 dBm with a DE and PAE of 20.1% and 15.3% (including all drivers), respectively. The 3 dB bandwidth was 0.9 GHz (1.2-2.1 GHz). The PA had a peak to minimum power ratio of ~40 dB.

Table I, published CMOS Class-D RF PAs are listed. The PA presented in this work has a 3.9 dB higher output power compared to previously published CMOS Class-D RF PAs.

B. Measured Performance of Modulated Signals

Table II presents the measured and required performance when uplink WCDMA and LTE signals were applied to the outphasing PA at 1.85 GHz. The channel powers of the WCDMA and LTE signals were +28.0 dBm and +24.9 dBm, respectively. The PAPR of the WCDMA and the LTE signal were 3.5 dB and 6.6 dB, respectively. The measured spectrums are shown in Fig. 8 and Fig. 9. Spectral and modulation requirements were met without requiring predistortion. The PAE was 4% when amplifying the LTE signal.

IV. Conclusions

This paper has presented a Class-D outphasing RF PA which can operate at a 5.5 V supply and deliver +32 dBm in a standard 130nm CMOS technology. The PA utilizes four on-chip transformers to combine the outputs of eight Class-D stages. The Class-D stages utilize a cascode configuration to allow a 5.5 V supply in the 1.2/2.5 V 130nm process without excessive device voltage stress. All transistors in the cascode configuration are driven by an AC-coupled 1.3 V driver. WCDMA and LTE (20 MHz, 16-QAM) signals were applied to the PA and for channel powers of +28.0 dBm and +24.9 dBm, respectively, the PA successfully met the spectral and modulation requirements.

To the authors’ best knowledge, the PA presented in this work has a 3.9 dB higher output power compared to previously published CMOS Class-D RF PAs.

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